REMARKS

The Office Action mailed July 12, 2005, has been received and reviewed. Claims 1 through 22 are currently pending in the application. Claims 1 through 5, 9 through 11, and 13 through 19 stand rejected. Claims 6 through 8, 12, and 20 through 22 have been objected to as being dependent upon rejected base claims, but the indication of allowable subject matter in such claims is noted with appreciation. Applicants have amended claims 1, 6, 9, 12, 15, and 20, and respectfully request reconsideration of the application as amended herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,486,005 to Kim in view of U.S. Patent No. 6,627,917 to Fenner et al.

Claims 1 through 4, 9, 11 and 13 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim (U.S. Patent No. 6,486,005) in view of Fenner et al. (U.S. Patent No. 6,627,917). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
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> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1 through 4, 9, 11 and 13 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Amended Independent Claim 1 and Dependent Claims 2-4

Regarding presently amended independent claim 1 and claims 2-4 at least indirectly depending therefrom, Applicants respectfully submit that any proposed combination of the Kim reference in view of the Fenner reference does not and cannot establish a prima facie case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of independent claim 1 and claims 2-4 depending therefrom because, at the very least, the cited prior art does not teach or suggest all the claim limitations of the presently claimed invention as set forth hereinabove.

Applicants' invention as presently claimed in independent claim 1 recites:

> 1. A semiconductor device, comprising:
> a first functional die including at least a first bond pad;
> at least a second functional die including at least a second bond pad, the at least a second functional die formed and maintained as a unitary integral wafer segment with the first functional die, ***the unitary integral wafer segment physically detached from any other wafer segments of a wafer***; and
> an adjacent die interconnection circuit operably coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die. (Emphasis added.)

In contrast, the Kim reference teaches or suggests:

> A fan-out type chip size package is efficiently fabricated at a level of wafer sized and stress buffer layers are formed at sides of the chip to rearrange bonding pads. (col. 3, lines 13-16)
> a first stress buffer layer 36 is formed at both sides of a unit semiconductor chip 31a, (col. 3, lines 19-20)
> the bonding pads 32 are formed on the upper part of the wafer 31 . . . [with] a first adhesive tape 33 . . . attached on the back of the wafer 31, . . . the scribe lane on the wafer 31 is then cut . . . to form unit semiconductor chips 31a and 31b. (col. 3, lines 48-56).

> Then, . . . the first adhesive tape 33 is expanded . . . [to] make the gap of the first cutting section 35 broaden . . . [then] a first stress buffer layer 36 is deposited on the whole surface including the first cutting section 35 . . . so that the semiconductor chips 31a and 31b are laterally supported. A material such as a silicon based benzocyclobutene (BCB), an oxide film or a nitride film is used as the first stress buffer layer 36, which acts as a buffer between chips and provides support. (col. 3, lines 57-67).

Clearly, the Kim reference teaches or suggests semiconductor chips individually formed on a wafer which are then individually separated from each other while attached to tape which can be stretched to expand the overall footprint of the wafer by increasing the spacing between each of the individually sectioned semiconductor chips. The spaces between the chips are then filled with material that in essence "glues the further-spaced apart chips back together for a lead forming process where the leads are formed on the newly deposited "stress buffer layer" deposited between the individual chips. The chips are then individually cut from each other by scribing them in the "glued" regions.

Nothing in Kim teaches or suggests integrated circuits including "***the at least a second functional die formed and maintained as a unitary integral wafer segment with the first functional die, the unitary integral wafer segment physically detached from any other wafer segments of a wafer***" as claimed by Applicants. Specifically, Kim does not teach "A semiconductor device, comprising: a first functional die including at least a first bond pad; at least a second functional die including at least a second bond pad, ***the at least a second functional die formed and maintained as a unitary integral wafer segment with the first functional die, the unitary integral wafer segment physically detached from any other wafer segments of a wafer***; and an adjacent die interconnection circuit operably coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die" as claimed in Applicants' amended independent claim 1.

The Office Action concedes that "Kim does not disclose that the at least a second functional die maintained as a unitary integral wafer segment with the first functional die." (Office Action. P. 2). The Office Action further alleges, "[h]owever, Fenner et al. disclose a semiconductor device comprising: a plurality of dice, wherein at least a second functional die

formed and maintained as a unitary integral wafer segment with a first functional die (figs. 1-2). (Office Action, p. 2).

A close reading of the Fenner et al. reference teaches or suggests:

> the [Fenner et al.] invention is directed to apparatus and methods for burn-in of dies while they are still part of the semiconductor wafer (i.e., burn-in at "wafer level") (col. 3, lines 41-43);
> the configuration of the conductors 204 preferably provides redundant interconnection between each die 200 and the pads 106 (col. 4, lines 50-52);
> [o]nce the supply 500 is connected to the r3espetive conductive pads 106 and activated, current is delivered to the respective die ponds pads 206 via the scribe conductors 204 (col. 7, lines 9-12);
> [w]hen the burn-in cycle is complete, the supply 500 is disconnected and the wafer 100 is partially singulated, e.g., partially sawn, along the scribe areas 105 to sever the conductors 204 (col. 7, lines 26-29);
> [a]t the completion of post bun-in testing, the dies 200 are singulated form the wafer 100 (col. 7, lines 44-45).

Clearly, neither the Kim reference nor the Fenner et al. reference, either individually or in any proper combination, teach or suggest Applicants' invention as claimed in presently amended independent claim 1, as neither reference teaches or suggests Applicants' claim limitation of "***the at least a second functional die formed and maintained as a unitary integral wafer segment with the first functional die, the unitary integral wafer segment physically detached from any other wafer segments of a wafer***".

Therefore, presently amended independent claim 1, and claims 2-4 depending therefrom, are not rendered obvious under 35 U.S.C. § 103 by the Kim reference in view of the Fenner et al. reference. Accordingly, such claims are allowable over the cited prior art and Applicants respectfully request that such rejections be withdrawn.

Amended Independent Claim 9 and Dependent Claims 11 and 13

Regarding presently amended independent claim 9 and claims 11 and 13 depending therefrom, Applicants respectfully submit that any proposed combination of the Kim reference in view of the Fenner reference does not and cannot establish a prima facie case of obviousness

under 35 U.S.C. § 103 regarding the presently claimed invention of independent claim 9 and claims 11 and 13 depending therefrom because, at the very least, the cited prior art does not teach or suggest all the claim limitations of the presently claimed invention as set forth hereinabove.

Applicants' invention as presently claimed in independent claim 9 recites:

> 9. A segment of a semiconductor wafer, comprising:
> two or more functional dice each including at least one bond pad, the two or more functional dice formed and maintained as a unitary integral wafer segment, ***the unitary integral wafer segment physically detached from any other wafer segments of the semiconductor wafer***; and
> an adjacent die interconnection circuit for mutually operably coupling each at least one bond pad of the two or more functional dice to at least one other bond pad of the two or more functional dice. (Emphasis added.)

Applicants sustain the above-recited teachings or suggestions of the Kim reference and the Fenner et al. reference. Furthermore, Applicants reiterate the above-proffered arguments relating to the teachings and suggestions of Kim reference and the Fenner et al. reference. Clearly, neither the Kim reference nor the Fenner et al. reference, either individually or in any proper combination, teach or suggest Applicants' invention as claimed in presently amended independent claim 9, as neither reference teaches or suggests Applicants' claim limitation of "***the unitary integral wafer segment physically detached from any other wafer segments of the semiconductor wafer***".

Therefore, presently amended independent claim 9, and claims 11 and 13 depending therefrom, are not rendered obvious under 35 U.S.C. § 103 by the Kim reference in view of the Fenner et al. reference. Accordingly, such claims are allowable over the cited prior art and Applicants respectfully request that such rejections be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 6,486,005 to Kim in view of U.S. Patent No. 6,627,917 to Fenner et al. and further in view of U.S. Patent No. 6,744,067 to Farnworth et al.

Claims 5, 10, and 14 through 19 stand rejected under 35 U.S.C. § 103(a) as being

unpatentable over Kim (U.S. Patent No. 6,486,005) in view of Fenner et al. (U.S. Patent No. 6,627,917) and further in view of Farnworth et al. (6,744,067). Applicants respectfully traverse this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
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> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 5, 10, and 14 through 19 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must teach or suggest all the claims limitations.

Dependent Claims 5, 10, and 14

The nonobviousness of presently amended independent claim 1 precludes a rejection of claim 5 which depends therefrom because a dependent claim is obvious only if the independent claim from which it depends is obvious. Similarly, the nonobviousness of presently amended independent claim 9 precludes a rejection of claims 10 and 14 which depend therefrom because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See* In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), *see also* MPEP § 2143.03.

Therefore, the Applicants request that the Examiner withdraw the 35 U.S.C. § 103(a) obviousness rejection to independent claims 1 and 9 and claim 5 and claims 10 and 14 which respectively depend therefrom.

Amended Independent Claim 15 and Dependent Claims 16-19

Regarding presently amended independent claim 15 and claims 16-19 at least indirectly depending therefrom, Applicants respectfully submit that any proposed combination of the Kim reference in view of the Fenner reference and further in view of the Farnworth et al. references does not and cannot establish a prima facie case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of independent claim 15 and claims 16-19 depending therefrom because, at the very least, the cited prior art does not teach or suggest all the claim limitations of the presently claimed invention as set forth hereinabove.

Applicants' invention as presently claimed in independent claim 15 recites:

> 15. A semiconductor wafer, comprising:
> a plurality of dice each including a bond pad, the plurality of dice segregated according to functional dice and nonfunctional dice; and
> an adjacent die interconnection circuit operably coupling a first bond pad of a first functional die with a second bond pad of a second functional die, the first functional die and the second functional die formed and maintained as a unitary integral independently functional segment of the semiconductor wafer, ***the unitary integral wafer segment physically detached from any other wafer segments of the semiconductor wafer***. (Emphasis added.)

Applicants sustain the above-recited teachings or suggestions of the Kim reference and the Fenner et al. reference. Furthermore, Applicants reiterate the above-proffered arguments relating to the teachings and suggestions of Kim reference and the Fenner et al. reference. The Office Action introduces the Farnworth reference and alleges:

> Farnworth et al. disclose that a first functional die and a second functional die are separated by at least one nonfunctional die (column 3, lines 28-30). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to test the device structure of Kim by having the nonfunctional die between the first and second functional dice, as taught by Farnworth et al., for testing of each individual die or groups of dice in order to determine and segregate operation dice from non functional die (column 8, lines 25-28). (Office Action , p. 4)

A closer reading of Farnworth states that "semiconductor die is fabricated according to conventional fabrication processes with each die including a defined number of die contacts that are electrically exposed for subsequent interconnection with other electronic components. One

embodiment of the [Farnworth] invention contemplates busing contacts of interest together from at least one die to at least one other die for wafer-level testing." (Col. 2, lines 30-37).

Clearly, neither the Kim reference nor the Fenner et al. reference nor the Farnworth et al. reference, either individually or in any proper combination, teach or suggest Applicants' invention as claimed in presently amended independent claim 15, as none of the references, either individually or in any proper combination, teach or suggest Applicants' claim limitation of "***the unitary integral wafer segment physically detached from any other wafer segments of the semiconductor wafer***".

Therefore, presently amended independent claim 15, and claims 16-19 depending therefrom, are not rendered obvious under 35 U.S.C. § 103 by the Kim reference in view of the Fenner et al. reference and further in view of the Farnworth et al. reference. Accordingly, such claims are allowable over the cited prior art and Applicants respectfully request that such rejections be withdrawn.

Objections to Claims 6-8, 12 and 20-22/Allowable Subject Matter

Claims 6 through 8, 12 and 20 through 22 stand objected to as being dependent upon rejected base claims, but are indicated to contain allowable subject matter and would be allowable if placed in appropriate independent form.

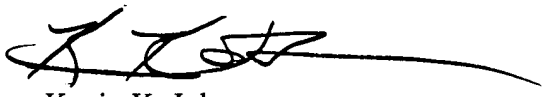
Accordingly, Applicants have amended claim 6 with claims 7 and 8 depending therefrom into independent form including all of the limitations of the base claim and any intervening claims. Similarly, Applicants have amended claim 12 into independent form including all of the limitations of the base claim and any intervening claims. Furthermore, Applicants have amended claim 20 with claims 21 and 22 depending therefrom into independent form including all of the limitations of the base claim and any intervening claims.

Applicants respectfully request the objections to claims 6 through 8, 12 and 20 through 22 be withdrawn.

CONCLUSION

Claims 1 through 22 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,



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